SOLID-STATE IMAGING DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2015-049365; filed March 12, 2015; the entire contents of which are incorporated herein by reference.

FIELD

Embodiments described herein relate generally to a solid-state imaging device.

BACKGROUND

In a solid-state imaging device including a plurality of pixels, a control circuit and a plurality of pixels are coupled to each other by wires, and each pixel is driven by signals which are supplied from the control circuit. At this time, it is preferable that time for driving each pixel is reduced.

An example of related art includes JP-A-2010-225927.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a sectional view illustrating a configuration of an imaging system to which a solid-state imaging device according to a first embodiment is applied.

FIG. 2 is a block diagram illustrating the configuration of the imaging system to which the solid-state imaging device according to the first embodiment is applied.

FIG. 3 is a circuit diagram illustrating the configuration of the solid-state imaging device according to the first embodiment.

FIG. 4 is a circuit diagram illustrating a configuration of a pixel according to a first embodiment.

FIG. 5 is an exploded perspective view illustrating a stacked structure of the solid-state imaging device according to the first embodiment.

FIG. 6 is a circuit diagram illustrating the stacked structure of the solid-state imaging device according to the first embodiment.

FIG. 7 is a circuit diagram illustrating a coupling configuration of a repeater and pixels according to a first embodiment.

FIG. 8 is a circuit diagram illustrating a stacked structure of a solid-state imaging device according to a modification example of the first embodiment.

FIG. 9 is a circuit diagram illustrating a stacked structure of a solid-state imaging device according to another modification example of the first embodiment.

FIG. 10 is a circuit diagram illustrating a stacked structure of a solid-state imaging device according to still another modification example of the first embodiment.

FIG. 11 is a circuit diagram illustrating a stacked structure of a solid-state imaging device according to still another modification example of the first embodiment.

FIG. 12 is a circuit diagram illustrating a stacked structure of a solid-state imaging device according to a second embodiment.

FIG. 13 is a circuit diagram illustrating a stacked structure of a solid-state imaging device according to a modification example of the second embodiment.

DETAILED DESCRIPTION

[0004]Exemplary embodiments provide a solid-state imaging device which can reduce time for driving each pixel.

[0005]According to one embodiment, a solid-state imaging device includes a first semiconductor chip and a second semiconductor chip. The first semiconductor chip includes a plurality of pixels. The first semiconductor chip is stacked on the second semiconductor chip. The second semiconductor chip includes an AD conversion circuit, a control circuit, a repeater line extending from the control line, a wire that three-dimensionally couples the repeater line to the plurality of pixels, and a plurality of repeaters that are disposed on the repeater line in correspondence with the plurality of pixels.

[0007]Solid-state imaging devices according to embodiments will be hereinafter described in detail with reference to the accompanying drawings. The present disclosure is not limited to the embodiments.

First Embodiment

[0008]A solid-state imaging device according to a first embodiment will be described. The solid-state imaging device is applied to, for example, an imaging system illustrated in FIG. 1 and FIG. 2. FIG. 1 and FIG. 2 are respectively a view and a diagram which illustrate a schematic configuration of the imaging system. OP of FIG. 1 represents an optical axis.

[0009]The imaging system 81 may be, for example, a digital camera, a digital video camera, or the like, and may be an electronic apparatus (for example, a camera-equipped mobile terminal or the like) to which a camera module is applied. The imaging system 81 includes an imaging unit 82 and a post processing unit 83 as illustrated in FIG. 2. The imaging unit 82 is, for example, a camera module. The imaging unit 82 includes an imaging optical system 84 and a solid-state imaging device 100. The post processing unit 83 includes an image signal processor (ISP) 86, a storage unit 87, and a display unit 88.

[0010]The imaging optical system 84 includes an imaging lens 47, a half mirror 49, a mechanical shutter 46, a lens 44, a prism 45, and a finder 48. The imaging lens 47 includes imaging lenses 47a and 47b, an aperture (not illustrated), and a lens drive mechanism 47c. The aperture is disposed between the imaging lens 47a and the imaging lens 47b, and adjusts an amount of light which is guided to the imaging lens 47b. In FIG. 1, an example in which the imaging lens 47 includes two imaging lenses 47a and 47b is illustrated, but the imaging lens 47 may include a plurality of imaging lenses.

[0011]The solid-state imaging device 100 is disposed in a predetermined imaging surface of the imaging lens 47. For example, the imaging lens 47 refracts incident light and can guide the light to an imaging surface of the solid-state imaging device 100 through the half mirror 49 and the mechanical shutter 46, and thereby an image of a subject is formed on the imaging surface of the solid-state imaging device 100. The solid-state imaging device 100 generates a pixel signal corresponding to image of the subject.

[0012]The solid-state imaging device 100 includes an image sensor 90, and a signal processing circuit 91, as illustrated in FIG. 3. FIG. 3 is a diagram illustrating a circuit configuration of the solid-state imaging device 100. The image sensor 90 may be, for example, a CMOS image sensor or a CCD image sensor. The image sensor 90 includes a pixel array PA, a row decoder 93, a timing control unit 95, a CDS+ADC 97, and a line memory 98.

[0013]The pixel array PA includes a plurality of pixels P which are arranged, for example, in a row direction and a column direction. The row decoder 93 controls the pixel array PA by, for example, a row unit in response to a control signal from the timing control unit 95.

[0014]As illustrated in FIG. 4, each pixel P includes, for example, a photoelectric conversion unit 3, a transfer unit 8, a charge voltage conversion unit 4, a reset unit 7, an amplification unit 5, and a select unit 6. FIG. 4 is a diagram illustrating a configuration of the pixel P. FIG. 4 exemplarily illustrates the pixel P(n,m) in an nth row and mth column, but the other pixels has the same configurations.

[0015]The photoelectric conversion unit 3 performs a photoelectric conversion, and generates and accumulates electric charges corresponding to the received light. The photoelectric conversion unit 3 includes, for example, a photo diode PD.

[0016]The transfer unit 8 transfers the electric charges of the photoelectric conversion unit 3 to the charge voltage conversion unit 4 in a state of activation, and does not transfer the electric charges of the photoelectric conversion unit 3 to the charge voltage conversion unit 4 in a state of deactivation. If receiving a control signal fREADn having an active level from the row decoder 93 through a drive line DL(n)-3, the transfer unit 8 transfers the electric charges of the photoelectric conversion unit 3 to the charge voltage conversion unit 4. If receiving the control signal fREADn having an inactive level from the row decoder 93 through a drive line DL(n)-3, the transfer unit 8 does not transfer the electric charges of the photoelectric conversion unit 3 to the charge voltage conversion unit 4. The transfer unit 8 includes, for example, a transfer transistor Td functioning as a transfer gate. If a gate of the transfer transistor receives the control signal fREADn having an active level, the transfer transistor is turned on, and thereby the electric charges of the photoelectric conversion unit 3 are transferred to the charge voltage conversion unit 4. If the gate of the transfer transistor receives the control signal fREADn having an inactive level, the transfer transistor is turned off, and thereby the electric charges of the photoelectric conversion unit 3 are not transferred to the charge voltage conversion unit 4.

[0017]The charge voltage conversion unit 4 converts electric charges which are transferred into a voltage using a parasitic capacitor thereof. The charge voltage conversion unit 4 includes, for example, a floating junction FJ.

[0018]The photoelectric conversion unit 3 starts accumulation of electric charges after transfer of the electric charges is completed by the transfer unit 8, and continues to accumulate the electric charges until the electric charges are subsequently transferred to the charge voltage conversion unit 4 by the transfer unit 8. That is, the photoelectric conversion unit 3 performs a charge accumulation operation, during a charge accumulation period from timing in which a transfer operation performed by the transfer unit 8 is completed to timing in which the subsequent transfer operation performed by the transfer unit 8 starts.

[0019]If receiving a control signal fRESET\_FJn having an active level from the row decoder 93 through a drive line DL(n)-2, the reset unit 7 resets a potential of the charge voltage conversion unit 4 to a predetermined potential (for example, VDDreset). The reset unit 7 includes, for example, a reset transistor Tc, and if a gate of the reset transistor receives the control signal fRESET\_FJn having an active level, the reset transistor Tc is turned on, and thereby the potential of the charge voltage conversion unit 4 is reset to a predetermined potential (for example, VDDreset).

[0020]The amplification unit 5 outputs a signal to a signal line SL on the basis of a voltage of the charge voltage conversion unit 4, when the pixel P(n,m) is in a selected state. The amplification unit 5 includes, for example, an amplification transistor Tb. When the pixel P(n,m) is in a selected state, the amplification unit 5 performs a source follower operation together with a load current source CS which is coupled to the amplification unit 5 through the signal line SL, and thereby a signal corresponding to a voltage of the charge voltage conversion unit 4 is output to the signal line SL. The load current source CS includes a load transistor TLM and a bias generation circuit 9.

[0021]If receiving a control signal fADRESn having an active level from the row decoder 93 through a drive line DL(n)-1, the select unit 6 makes the pixel P(n,m) be in a selected state, and if receiving the control signal fADRESn having an inactive level from the row decoder 93 through a drive line DL(n)-1, the select unit 6 makes the pixel P(n,m) be in a non-selected state. The select unit 6 includes, for example, a select transistor Ta. When a gate of the select transistor receives the control signal fADRESn having an active level, the select transistor is turned on, and thereby the select unit 6 makes the pixel P9(n,m) be in a selected state. When the gate of the select transistor receives the control signal fADRESn having an inactive level, the select transistor is turned off, and thereby the select unit 6 makes the pixel P9(n,m) be in a non-selected state. A drain of the select transistor Ta is coupled to a power supply potential VDDsf. The power supply potential VDDsf can be shorted to the power supply potential VDDreset.

[0022]FIG. 4 illustrates a configuration in which the select transistor Ta is coupled o the power supply potential VDDsf and the amplification transistor Tb is coupled to the signal line SL. A configuration in which the amplification transistor Tb is coupled to the power supply potential VDDsf and the select transistor Ta is coupled to the signal line SL may be used.

[0023]In addition, the pixel P may have a configuration in which the select unit 6 is omitted. In this case, the drive line DL(n)-1 may be omitted, and the reset unit 7 may perform an operation of making the pixel P be in a selected state of a non-selected state. For example, the reset unit 7 may reset the potential of the charge voltage conversion unit 4 to a first potential (for example, VDD level) and thereby the pixel P is in a selected state, and the reset unit 7 may reset the potential of the charge voltage conversion unit 4 to a second potential (potential by which the amplification unit 5 (the amplification transistor Tb) is turned off, for example, ground level) and thereby the pixel P is in a non-selected state.

[0024]Each pixel P includes a plurality of drive lines DL(n) which extend, but hereinafter, for the sake of a brief description, it is assumed that each pixel P includes one drive line DL(n) which extends. In addition, each pixel P receives a plurality of control signals, but for the sake of a brief description, it is assumed that each pixel P receives one control signal.

[0025]Returning to FIG. 3, pixel signals which are generated by each pixel P are read to the CDS+ADC 97 by the timing control unit 95 and the row decoder 93, are converted into image data through the CDS+ADC 97, and are output to the signal processing circuit 91 through the line memory 98. The signal processing circuit 91 performs signal processing. The image data which is obtained by performing signal processing is output to the ISP 86.

[0026]As illustrated in FIG. 3 and FIG. 4, the row decoder 93 is disposed in the periphery of the pixel array PA, and each drive line DL extends in a row direction to each pixel in a corresponding row from the row decoder 93. The row decoder 93 sequentially selects the first row, the second row,… to be driven, among the plurality of rows of the pixel array PA, and supplies a control signal to the plurality of pixels included in the selected rows of the pixel array PA through a drive line DL in the selected row.

[0027]For example, if the pixel array PA includes many pixels in order to meet the requirement of an increasing number of pixels, the drive line DL becomes long, and thereby resistance of the drive line DL easily increases. In addition, since the number of pixels which are coupled to the drive line DL increases, capacitance of the drive line DL easily increases. For this reason, when the row decoder 93 drives the pixels through the drive line DL, a pixel driving time may increase.

[0028]If the pixel driving time increases, it may not possible to satisfy the speed that is required by a frame rate of the pixel signal which is output from the solid-state imaging device 100. If the speed that is required by the frame rate is not satisfied, it is difficult to ensure the number of frames within a predetermined time, and to obtain a smooth moving image, in a case in which an image that is obtained by an image signal is a moving image. Alternatively, in a case in which the image that is obtained by the image signal is a still image, a release time lag increases, and it may be difficult to capture an image.

[0029]At this time, it is difficult to reduce a resistance and a capacitance of the drive line DL, in order to ensure pixel characteristics. It is considered a case in which a repeater for driving a control signal is inserted between the row decoder 93 on the drive line DL and the pixel array PA. In this case, the inserted repeater drives the plurality of pixels coupled to the drive line DL from one end of the drive line DL, and thus the repeater is greatly affected by delay due to the capacitance. For this reason, it may be difficult to reduce the pixel driving time.

[0030]In addition, since the pixel array PA ensures pixel characteristics (pixel arrangement pitch), it is difficult to add the repeater at a position between the pixels on the drive line DL.

[0031]However, in the first embodiment, a junction of the electrodes can be disposed under the pixel area by a chip stacked structure using substrate bonding, a plurality of repeaters are inserted into a position corresponding to a plurality of pixels in a repeater line of a lower chip, and the control signal which is driven is supplied from the lower chip to an upper chip, and thus the delay of the control signal decreases.

[0032]Specifically, the solid-state imaging device 100 includes a semiconductor chip CH1 and a semiconductor chip CH2, as illustrated in FIG. 5 and FIG. 6. FIG. 5 is an exploded perspective view illustrating a stacked structure of the solid-state imaging device 100. FIG. 6 illustrates a circuit diagram illustrating a stacked structure of the solid-state imaging device 100.

[0033]The semiconductor chip CH1 is stacked on the semiconductor chip CH2. The semiconductor chip CH1 and the semiconductor chip CH2 are bonded by substrate bonding. A substrate of the semiconductor chip CH1 can be bonded to a substrate of the semiconductor chip CH2, and electrodes EL thereof can be bonded together (for example, Cu-Cu bonding). The semiconductor chip CH1 and the semiconductor chip CH2 respectively have multilayer wiring structures on surfaces thereof, and respectively have the electrodes EL whose surfaces are exposed on top wiring layers thereof.

[0034]The pixel array PA of the configuration elements of the solid-state imaging device 100 illustrated in FIG. 3 is disposed on the semiconductor chip CH1. For example, the semiconductor chip CH1 includes a plurality of pixels P(1,1) to P(4,4), a plurality of drive lines DL(1) to DL(4), a plurality of wires WR(1,1) to WR(4,4), and a plurality of signal lines (not illustrated). The plurality of pixels P(1,1) to P(4,4) are arranged in a row direction and a column direction, for example, configures four rows and four columns. In FIG. 5, and FIG. 6, a case in which the arranged number of pixels in the pixel array PA is four rows and four columns is exemplified, but the arranged number of pixels is not limited to this. The plurality of pixels P(1,1) to P(4,4) has a pixel structure of a backside illumination type (not illustrated).

[0035]The plurality of drive lines DL(1) to DL(4) correspond to the plurality of pixel rows. The respective drive lines DL(1) to DL(4) extend in a row direction, and are coupled to each pixel of the corresponding rows. For example, the drive line DL(1) corresponds to the pixels P(1,1) to P(1,4) in the first row, and is coupled to the pixels P(1,1) to P(1,4) in the first row.

[0036]Each of the plurality of wires WR(1,1) to WR(4,4) three-dimensionally couples the drive lines DL(1) to DL(4) to the semiconductor chip CH2. For example, the wires WR(1,1) to WR(1,4) respectively couples nodes DN(1,1) to DN(1,4) on the drive line DL(1) to the electrodes EL provided thereunder.

[0037]Portions other than the pixel array PA among the configuration elements of the solid-state imaging device 100 illustrated in FIG. 3 are disposed on the semiconductor chip CH2. For example, the semiconductor chip CH2 includes an ADC 97, a logic circuit 99, a row decoder (control circuit) 93, a plurality of repeater lines RL(1) to RL(4), a plurality of wires LWR(1,1) to LWR(4,4), and a plurality of repeaters RP(1,1) to RP(4,4). In the semiconductor chip CH2, the row decoder 93 is disposed in the vicinity of an end portion. ADC disposition areas 11 to 14 and logic circuit disposition areas 15 to 18 are provided in the vicinity of a disposition area of the row decoder 93. For example, the ADC 97 is disposed in a divided manner in the ADC disposition areas 11 to 14. The logic circuit 99 is disposed in a divided manner in the logic circuit disposition areas 15 to 18. The logic circuit 99 includes the signal processing circuit 91 and the like (refer to FIG. 3).

[0038]The plurality of repeater lines RL(1) to RL(4) correspond to the plurality of drive lines DL(1) to DL(4). Each of the repeater lines RL(1) to RL(4) extends along the corresponding drive line DL. For example, the repeater lines RL(1) and RL(2) extend in a row direction from the row decoder 93, and penetrate the logic circuit disposition areas 15 to 18. The repeater lines RL(1) and RL(2) penetrate the logic circuit disposition areas 15 to 18, but are not coupled to the logic circuit 99. For example, the repeater lines RL(3) and RL(4) extend in a row direction from the row decoder 93, and penetrate the ADC disposition areas 11 to 14. The repeater lines RL(3) and RL(4) penetrate the ADC disposition areas 11 to 14, but are not coupled to the ADC 97.

[0039]Each of the plurality of wires LWR(1,1) to LWR(4,4) three-dimensionally couples the repeater lines RL(1) to RL(4) to the semiconductor chip CH1. For example, the wires LWR(1,1) to LWR(1,4) respectively couple nodes RN(1,1) to RN(1,4) on the repeater line RL(1) to the electrodes EL provided thereon.

[0040]For example, coupling is made in a sequence of node RN(1,1)®wire LWR(1,1)®electrode EL of semiconductor chip CH2®electrode EL of the semiconductor chip CH1®wire WR(1,1)®node DN(1,1)®pixel P(1,1). In addition, coupling is made in a sequence of node RN(1,4)®wire LWR(1,4)®electrode EL of semiconductor chip CH2®electrode EL of the semiconductor chip CH1®wire WR(1,4)®node DN(1,4)®pixel P(1,4). That is, each of the plurality of wires LWR(1,1) to LWR(4,4) three-dimensionally couples the repeater lines RL(1) to RL(4) to the plurality of pixels.

[0041]The plurality of repeaters RP(1,1) to RP(4,4) correspond to the plurality of repeater lines RL(1) to RL(4). The plurality of repeaters RP(1,1) to RP(1,4) are disposed on the repeater line RL(1) so as to correspond to the plurality of pixels P(1,1) to P(1,4). The plurality of repeaters RP(1,1) to RP(1,4) can drive the pixels P(1,1) to P(1,4) in the same row of the pixel array PA.

[0042]For example, an input terminal of the repeater RP(1,1) is coupled to the row decoder 93 through the repeater line RL(1), as illustrated in FIG. 7. FIG. 7 is a circuit diagram illustrating a coupling configuration of the repeaters and the pixels. An output terminal of the repeater RP(1,1) is coupled to the pixel P(1,1) through the repeater line RL(1), the wire LWR(1,1), and WR(1,1), and is coupled to an input terminal of the repeater RP(1,2) of a subsequent stage through the repeater line RL(1). Accordingly, the repeater RP(1,1) can drive a control signal to the pixel P(1,1), and at the same time, can also drive a control signal to the repeater RP(1,2) of a subsequent stage.

[0043]An input terminal of the repeater RP(1,2) is coupled to the repeater RP(1,1) through the repeater line RL(1). An output terminal of the repeater RP(1,2) is coupled to the pixel P(1,2) through the repeater line RL(1), the wire LWR(1,2), and WR(1,2), and is coupled to an input terminal of the repeater RP(1,3) of a subsequent stage through the repeater line RL(1). Accordingly, the repeater RP(1,2) can drive a control signal to the pixel P(1,2), and at the same time, can also drive a control signal to the repeater RP(1,3) of a subsequent stage.

[0044]An input terminal of the repeater RP(1,3) is coupled to the repeater RP(1,2) through the repeater line RL(1). An output terminal of the repeater RP(1,3) is coupled to the pixel P(1,3) through the repeater line RL(1), the wire LWR(1,3), and WR(1,3), and is coupled to an input terminal of the repeater RP(1,4) of a subsequent stage through the repeater line RL(1). Accordingly, the repeater RP(1,3) can drive a control signal to the pixel P(1,3), and at the same time, can also drive a control signal to the repeater RP(1,4) of a subsequent stage.

[0045]An input terminal of the repeater RP(1,4) is coupled to the repeater RP(1,3) through the repeater line RL(1). An output terminal of the repeater RP(1,4) is coupled to the pixel P(1,4) through the repeater line RL(1), the wire LWR(1,4), and WR(1,4). Accordingly, the repeater RP(1,4) can drive a control signal to the pixel P(1,4).

[0046]In the same manner, the plurality of repeaters RP(4,1) to RP(4,4) are disposed on the repeater line RL(4) so as to correspond to the plurality of pixels P(4,1) to P(4,4). The plurality of repeaters RP(4,1) to RP(4,4) can drive the pixels P(4,1) to P(4,4) in the same row of the pixel array PA.

[0047]As described above, in the first embodiment, in the solid-state imaging device 100, a junction of the electrodes can be disposed under the pixel area by a chip stacked structure using substrate bonding, the plurality of repeaters are inserted into a position corresponding to the plurality of pixels in a repeater line of the lower chip, and the control signal which is driven is supplied from the lower chip to the upper chip. Accordingly, the control signal can be driven in the middle of a path of the control signal from the row decoder 93 to the pixel, and thus it is possible to easily reduce the delay of the control signal and to easily reduce the pixel driving time, compared to a case in which the control signal is driven from one terminal of the drive line DL. As a result, it is possible to achieve a high speed of the frame rate, and to satisfy the speed which is required for the frame rate.

[0048]In addition, in the first embodiment, in the solid-state imaging device 100, for example, the repeaters RP(1,1) to RP(1,3) can drive the control signal to the pixels P(1,1) to (1,3), and at the same time, can also drive the control signal to the repeaters RP(1,2) to RP(1,4) of a subsequent stage. Accordingly, it is possible to decrease driving capability of each of the repeaters RP(1,1) to RP(1,3), and to easily reduce the delay of the control signal, compared to a case in which the drive signal is driven from one terminal of the drive line DL. In addition, since the pixels far from the row decoder 93 are also repeatedly driven, it is possible to reduce a difference of a waveform distortion of the control signal between the pixel P(1,1) close to the row decoder 93 and the pixel P(1,4) far from the row decoder 93. Furthermore, the control signal is transferred through a common repeater line RL(1) to the pixel P(1,1) close to the row decoder 93 and the pixel P(1,4) far from the row decoder 93, and thus it is possible to decrease wiring density of the repeater line RL(1), and to easily thicken the repeater line RL(1) such that a wiring resistance of the repeater line RL(1) does not increase.

[0049]The repeaters RP corresponding to each pixel are disposed on each repeater line RL, but the repeaters RP corresponding to a plurality of pixels may be disposed.

[0050]The drive line DL in each row of the semiconductor chip CH1 may be divided for each repeater RP. For example, in the drive line DL(1) in the first row illustrated in FIG. 6, the drive line DL(1) in the first row may be divided into a plurality of drive lines DL(1)\_1 to DL(1)\_4 by cutting dashed lines, as illustrated in FIG. 8. FIG. 8 is a circuit diagram illustrating a stacked structure of a solid-state imaging device 100i according to a modification example of the first embodiment. Drive lines in the other rows may also be configured in the same manner. Accordingly, for example, the number of the pixels P which is coupled to the drive line DL coupled to each repeater RP can be reduced to one piece, and thus it is possible to effectively reduce the capacitance value of the drive line DL of the solid-state imaging device 100i, and to easily reduce the delay of the control line of the solid-state imaging device 100i.

[0051]Alternatively, the row decoder of the semiconductor chip CH2 may drive the control line at both ends of the repeater line. For example, as illustrated in FIG. 9, a row decoder 93’ may be coupled to a side opposite to the row decoder 93 of each of the repeater lines RL(1) to RL(4). FIG. 9 is a circuit diagram illustrating a stacked structure of a solid-state imaging device 100j according to another modification example of the first embodiment. For example, the row decoder 93 can drive the pixel P(1,1) and P(1,2) through repeaters RP(1,1) and RP(1,2), the wires LWR(1,1) and LWR(1,2), and WR(1,1) and WR(1,2). For example, the row decoder 93’ can drive the pixel P(1,4) and P(1,3) through repeaters RP(1,4) and RP(1,3), the wires LWR(1,4) and LWR(1,3), and WR(1,4) and WR(1,3). In this way, the pixels in each row can be driven at both ends of the drive line, and thus it is possible to increase drive capability of the control line of the solid-state imaging device 100j and to further reduce the delay of the control line of the solid-state imaging device 100j.

[0052]Alternatively, as illustrated in FIG. 9, the repeater lines RL in each row of the semiconductor chip CH2 may be divided for each of the row decoders 93 and 93’. For example, in the repeater line RL(1) in the first row illustrated in FIG. 9, the repeater line RL(1) in the first row may be divided into a plurality of repeater lines RL(1)\_1 and RL(1)\_2 by cutting dashed line, as illustrated in FIG. 10. FIG. 10 is a circuit diagram illustrating a stacked structure of a solid-state imaging device 100k according to still another modification example of the first embodiment. The drive lines in the other rows may be configured in the same manner. Accordingly, for example, the number of the repeater lines RP which are coupled to the repeater lines RL coupled to each of the row decoders 93 and 93’ can be reduced to half, and thus it is possible to effectively reduce the capacitance value of the repeater line RL of the solid-state imaging device 100k, and to easily reduce the delay of the control line of the solid-state imaging device 100k.

[0053]Alternatively, in the configuration illustrated in FIG. 10, the drive lines DL in each row of the semiconductor chip CH1 may be divided for each repeater RP. For example, in the drive line DL(1) in the first row illustrated in FIG. 10, the drive line DL(1) in the first row may be divided into a plurality of drive lines DL(1)\_1 to DL(1)\_4 by cutting dashed line, as illustrated in FIG. 11. FIG. 11 is a circuit diagram illustrating a stacked structure of a solid-state imaging device 100p according to still another modification example of the first embodiment. The drive lines in the other rows may be configured in the same manner. Accordingly, for example, the number of the pixels P which are coupled to the drive lines DL coupled to each repeater RP can be reduced to one piece, and thus it is possible to effectively reduce the capacitance value of the drive line DL of the solid-state imaging device 100p, and to easily reduce the delay of the control line of the solid-state imaging device 100p.

Second Embodiment

[0054]Subsequently, a solid-state imaging device 200 according to a second embodiment will be described. Hereinafter, description will be made by focusing on portions different from the first embodiment.

[0055]In the first embodiment, the control signal which is output from the row decoder 93 and is driven by the repeater RP is supplied to the pixel P through the wires LWR and WR, and thereby the pixel P is driven.

[0056]However, in order to reduce power consumption or the like, operation voltages of the row decoder 93 and the repeater RP decrease, and a case in which the level of the control signal which is supplied to the pixel P is not sufficient for the required level as it is may occur. For example, if an active level of the control signal fREADn is relatively low, when the transfer unit 8 is turned on and thereby the electric charges of the photoelectric conversion unit 3 are transferred to the charge voltage conversion unit 4, an afterimage caused by partial electric charges which remain in the photoelectric conversion unit 3 without being transferred can occur.

[0057]However, in the second embodiment, the control signal which is output from the row decoder 93 and is driven by the repeater RP is converted into a signal with a desired voltage amplitude (desired level) before being supplied to the pixel P.

[0058]Specifically, as illustrated in FIG. 12, a semiconductor chip CH202 further includes a plurality of level shifters LS(1,1) to LS(4,4). FIG. 12 is a circuit diagram illustrating a stacked structure of the solid-state imaging device 200. The plurality of level shifters LS(1,1) to LS(1,4) are disposed on the wires LWR(1,1) to LWR(1,4) so as to correspond to the plurality of pixels P(1,1) to P(1,4). The plurality of level shifters LS(1,1) to LS(1,4) can drive the pixels P(1,1) to P(1,4) in the same rows of the pixel array PA.

[0059]For example, the level shifter LS(1,1) is disposed on the wire LWR(1,1). If an amplitude of the control signal which is driven by the repeater RP(1,1) which is output from the row decoder 93 is V1, the level shifter LS(1,1) converts the amplitude of the control signal from V1 to V2 (>V1). The level shifter LS(1,1) supplies the control signal whose amplitude is converted into V2 to the pixel P(1,1) through the wires LWR(1,1) and WR(1,1). Accordingly, the pixel P(1,1) can be driven by a control signal with a desired level.

[0060]The level shifter LS(1,4) is disposed on the wire LWR(1,4). If an amplitude of the control signal which is driven by each of the repeaters RP(1,1) to RP(1,4) which are output from the row decoder 93 is V1, the level shifter LS(1,4) converts the amplitude of the control signal from V1 to V2 (>V1). The level shifter LS(1,4) supplies the control signal whose amplitude is converted into V2 to the pixel P(1,4) through the wires LWR(1,4) and WR(1,4). Accordingly, the pixel P(1,4) can be driven by a control signal with a desired level.

[0061]As described above, in the second embodiment, in the solid-state imaging device 200, the control signal which is output from the row decoder 93 and is driven by the repeater RP is converted into a desired voltage amplitude (desired level) by the level shifter LS before being supplied to the pixel P. Accordingly, if operation voltages of the row decoder 93 and the repeater RP decrease in order to reduce power consumption or the like, it is possible to drive the pixel P using a control signal with a desired level, and to improve the characteristics of the pixel P.

[0062]The level shifter may be disposed on each repeater line RL instead of being disposed on each wire LWR. For example, as illustrated in FIG. 13, in a solid-state imaging device 200’, a semiconductor chip CH202’ may include a plurality of level shifters LS’(1) to LS’(4). FIG. 13 is a circuit diagram illustrating a stacked structure of the solid-state imaging device. The level shifters LS’(1) to LS’(4) are disposed between the row decoder 93 and the plurality of repeaters RP on the repeater lines RL(1) to RL(4).

[0063]For example, the level shifter LS’(1) is disposed between the row decoder 93 and the plurality of repeaters RP(1,1) to RP(1,4) on the repeater line RL(1). If the amplitude of the control signal which is output from the row decoder 93 is V1, the level shifter LS’(1) converts the amplitude of the control signal from V1 to V2 (>V1). The level shifter LS’(1) supplies the control signal whose amplitude is converted into V2 to the pixel P(1,1) through the repeater line RL(1), the repeater RP(1,1), and the wires LWR(1,1) and WR(1,1). Accordingly, it is possible to drive the pixel P(1,1) using a control signal with a desired level.

[0064]In this way, if the level shifter LS’ is disposed between the row decoder 93 and the plurality of repeaters RP on each repeater line RL instead of being disposed on each wire LWR, it is possible to reduce the number of the level shifters LS’ to be prepared, and to reduce cost for the solid-state imaging device 200’.

[0065]While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

WHAT IS CLAIMED IS:

1. A solid-state imaging device comprising:

a first semiconductor chip which includes a plurality of pixels; and

a second semiconductor chip on which the first semiconductor chip is stacked, and which includes an AD conversion circuit, a control circuit, a repeater line extending from the control line, a wire that three-dimensionally couples the repeater line to the plurality of pixels, and a plurality of repeaters that are disposed on the repeater line in correspondence with the plurality of pixels.

2. The device according to Claim 1,

wherein the plurality of pixels includes:

a first pixel; and

a second pixel, and

wherein the plurality of repeaters includes:

a first repeater which has an input terminal that is coupled to the control circuit through the repeater line, and an output terminal that is coupled to the first pixel through the repeater line and the wire; and

s second repeater which has an input terminal that is coupled to the output terminal of the first repeater through the repeater line, and an output terminal that is coupled to the second pixel through the repeater line and the wire.

3. The device according to Claim 1 or 2,

wherein the plurality of pixels are disposed at least in a row direction,

wherein the repeater line extends in a row direction, and

wherein the wire three-dimensionally couples the repeater line to a plurality of pixels in the same row.

4. The device according to any one of Claims 1 to 3, wherein the second semiconductor chip further includes a plurality of level shifters which are disposed on the wire so as to correspond to the plurality of pixels.

5. The device according to any one of Claims 1 to 3, wherein the second semiconductor chip further includes a level shifter which is disposed between the control circuit on the repeater line and the plurality of repeaters.

ABSTRACT

A solid-state imaging device according to an embodiment includes a first semiconductor chip and a second semiconductor chip. The first semiconductor chip includes a plurality of pixels. The first semiconductor chip is stacked on the second semiconductor chip. The second semiconductor chip includes an AD conversion circuit, a control circuit, a repeater line extending from the control line, a wire that three-dimensionally couples the repeater line to the plurality of pixels, and a plurality of repeaters that are disposed on the repeater line in correspondence with the plurality of pixels.

Drawings

FIG. 2

82: IMAGING UNIT

84: IMAGING OPTICAL SYSTEM

100: SOLID-STATE IMAGING DEVICE

81: IMAGING SYSTEM

83: POST PROCESSING UNIT

87: STORAGE UNIT

88: DISPLAY UNIT

FIG. 3

90: IMAGE SENSOR

95: TIMING CONTROL UNIT

93: ROW DECODER

PA: PIXEL ARRAY

98: LINE MEMORY

100: SOLID-STATE IMAGING DEVICE

91: SIGNAL PROCESSING CIRCUIT

FIG. 4

9: BIAS GENERATION CIRCUIT

TO CDS+ADC 97

FIG. 5

93: ROW DECODER

FIG. 6

93: ROW DECODER

FIG. 7

ROW DECODER

P(1,1): PIXEL

SAME ROW

FIG. 8

93: ROW DECODER

FIG. 9

93: ROW DECODER

93’: ROW DECODER

FIG. 10

93: ROW DECODER

93’: ROW DECODER

FIG. 11

93: ROW DECODER

93’: ROW DECODER

FIG. 12

93: ROW DECODER

FIG. 13

93: ROW DECODER